Preliminary

SME2411

SUN MICROELECTRONICS

July 1997

UltraSPARC™-IIi APB

DATA SHEET Advanced PCI Bridge, 66-MHz-Primary-to-33-MHz-Secondary

FUNCTIONAL DESCRIPTION

The Advanced PCI Bridge (APB™), SME2411, is a PCI-to-PCI bridge chip that is compatible with version 2.1 of the *PCI Local Bus Specification* [1]. The APB features a connection path between a 32-bit bus running at speeds up to 66 MHz on the *primary interface* and two 32-bit, 5 V or 3.3 V, PCI buses (each running up to 33 MHz), on the *secondary interface*. It is primarily intended as an interconnect mechanism, for use in an UltraSPARC-II*i*-based system.

The APB provides the UltraSPARC-II*i* microprocessor direct access, with minimum latency, to devices located on a connected PCI bus and mapped in the processor's I/O or memory address space. In addition, it provides PCI masters direct, high-capacity access to main memory. Use of the APB depends upon the organization of the PCI bus.

The Advanced PCI Bridge features are shown in the list entitled "Features," on page 2. "Benefits of the Advanced PCI Bridge," on page 3 and "Benefits of UltraSPARC-IIi with the Advanced PCI Bridge," on page 3 discuss advantages which can be realized in systems employing these two devices. *Figure 29* shows how the APB provides expanded PCI capability to an UltraSPARC-II*i*-based system. *Figure 30* shows an example of system implementation.

The entire PCI domain is viewed as non-cacheable by UltraSPARC-II*i*. Coherent DMA is supported (in other words, all writes to memory from PCI and reads from memory to PCI are cache-coherent).

1. All references to the PCI specification refer to *PCI Local Bus Specification Revision 2.1*, June 1, 1995.

Features

- 32-Bit PCI Revision 2.1 Compatible [1]
- PCI Bridge Specification 1.0 Compatible [1]
- 32-Bit Memory Addressing for PIO and DMA
- 64-Bit Memory Addressing (DACs) for DMA
- 24-Bit I/O Addressing (PIO only)
- Full Concurrency for Primary and Secondary PCI Interfaces
  - Uses Deadlock Detection / Recovery Mechanism
- Data Buffering
  - A 72-Byte Buffer (FIFO) on each of the DMA and PIO Paths
- Two On-Chip Programmable Arbiters
  - One for each Secondary PCI Interface
  - Each One Handles up to 4 Secondary Bus Masters
  - Priority to each Master is Programmable, so any Master can be Given Priority
- External Arbiters for Secondary PCI Buses Allowed
- Retry Counters and Latency Timers can be Configured for Differing Performance Requirements
- Prefetching for some Memory Read Commands
- Prefetching Algorithm can be Varied for DMA
- Interrupt Handling
  - Synchronization Mechanism for DMA Writes
  - PCI Interrupts are Routed through an External Interrupt Concentrator
- PCI Optional Features Implemented [2]
  - Fast Back-to-Back Capable as a Target
  - Medium Decode Timing
- Boot Mode Allows APB to Be Used in the Path of the Boot PROM
- Transactions Originating on One Secondary Bus Cannot Be Destined for Targets on the Other
- Little-Endian to the Bus and Internal Configuration Space
- Errors Resulting in Assertion of SERR# Are Logged
- PIO Reads and Writes are in Non-Cacheable Memory Space (When Used with UltraSPARC-II*i*)

1. See "Exceptions to PCI Compatibility," on page 13.
2. See "PCI Optional Features Not Implemented," on page 13.

Benefits of the Advanced PCI Bridge

- The Advanced PCI Bridge expands available system slots.
- The Primary 66-MHz bus provides a high- bandwidth path through the CPU to main memory.
- Concentrating two 33-MHz busses onto one 66-MHz allows two 33-MHz devices to achieve high DMA write bandwidth simultaneously.
- Relaxation of PCI ordering rules improves performance -- reads do not have to wait for opposing posted writes to complete.
- Read prefetching gives higher read performance.
- BOOT mode pin enables APB at reset, allowing boot PROMs to be located behind APB.
- APB can be used in 33 MHz to 33 MHz mode, allowing hierarchical configurations.
- Error logging capabilities, including the address of any error signalled by APB.
- APB can be used to generate interrupt-acknowledge transactions (INT ACK cycles), allowing standard PCI-to-ISA (“south“) bridges to be used with CPU/host bridge combinations that are not able to generate INT ACKs.
- APB routes INT ACK cycles received on the primary bus to either secondary bus, allowing PC-standard south bridges to exist on the secondary bus instead of the primary bus.
- APB includes a timer-register that can be used as a fixed-frequency counter.
- Non-enforcement of optional latency limits improves performance. [1]

Benefits of UltraSPARC-IIi with the Advanced PCI Bridge

- Used with UltraSPARC-II*i*, APB provides a dynamic pipeline from the secondary bus devices to main memory for high performance.
- APB’s ability to accept 5 V secondary bus devices allows 5 V commodity devices to be used with UltraSPARC-II*i*.
- Dedicated signals allow DMA synchronization with no performance degradation due to synchronization transactions.
-

1. Default operation of the APB does not enforce latency limits specified in the PCI specification, revision 2.1. Systems involving no peer-to-peer communication realize no benefits from enforced latency limits, which also cause additional deadlock possibilities and power consumption. However, target latency-limit registers are provided, and these can be programmed to enforce the limits in the PCI specification.

TABLE 1: Key Terminology for APB

Term	Usage
DAC	Dual address cycle.
Datapath	A target and master block pair with a FIFO between them. There are four datapaths in APB: PIO-A, PIO-B, DMA-A, and DMA-B.
Destination	The bus containing the final target for a transaction.
DMA	Accesses by a master on the secondary bus to a target on the primary bus. Equivalent to “upstream”.
Downstream	Accesses by a master on the primary bus to a target on the secondary bus. Equivalent to “PIO”.
Master	An agent that initiates transactions.
Master Block	A block within APB that can initiate transactions.
Originating	The bus containing the original master for a transaction.
PIO	Accesses by a master on the primary bus to a target on the secondary bus. Equivalent to “downstream”.

TABLE 1: Key Terminology for APB (Continued)

Term	Usage
Probing Algorithm	The algorithm used by configuration software to detect PCI devices, assign address spaces, and configure bridges.
Target	An agent that responds to a transaction.
Target Block	A block within APB which responds to transactions.
Upstream	Accesses by a master on the secondary bus to a target on the primary bus. Equivalent to “DMA”.

Block Diagram

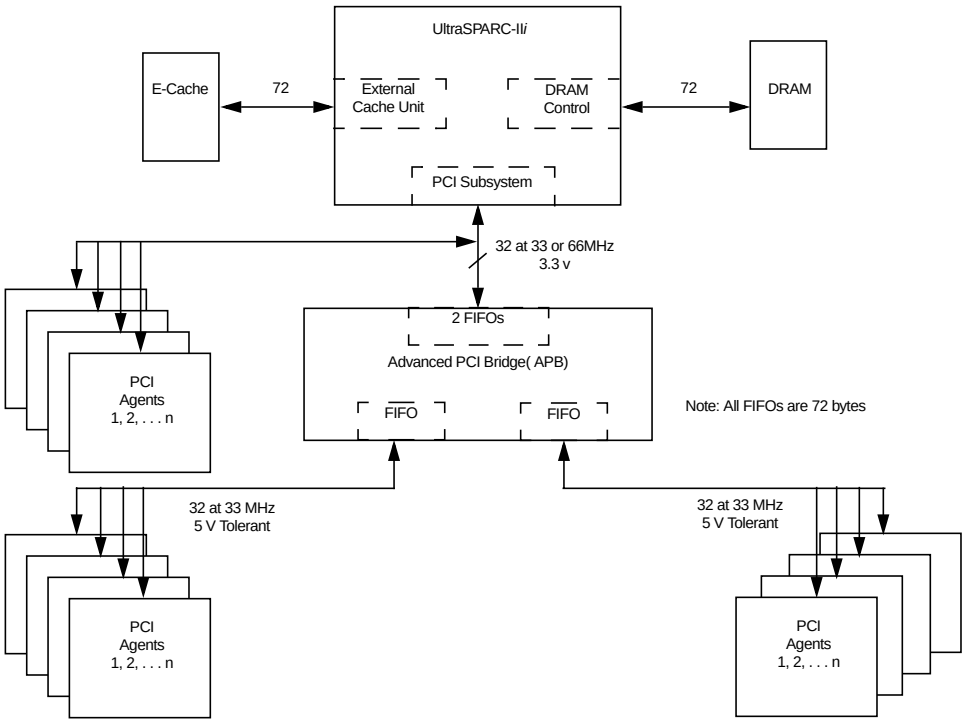


Figure 29. PCI Connectivity in an UltraSPARC-II*i* System

System Illustration

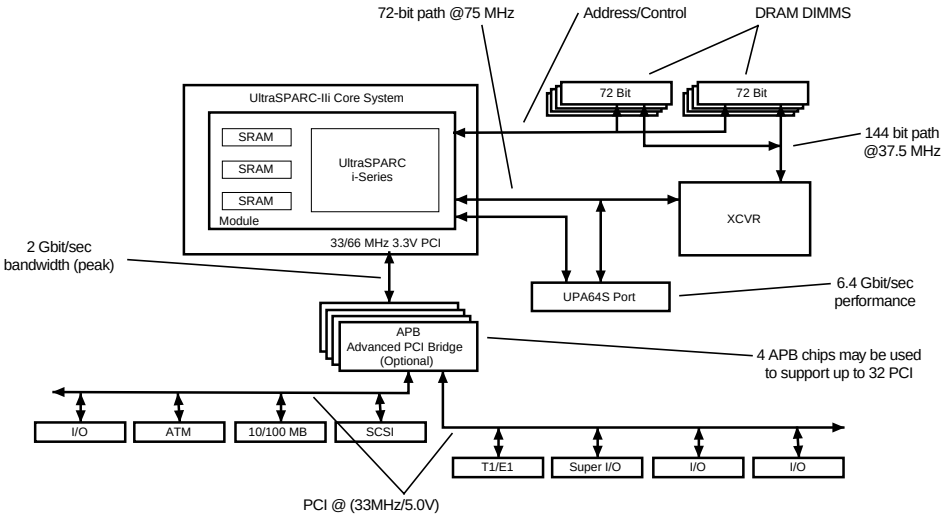


Figure 30. APB System Implementation Example

Data Path Overview

Figure 31 below shows the major datapaths and modules in the Advanced PCI Bridge.

The APB has two pair of PIO and DMA FIFOs, one for the each of the possible datapaths between the primary interface and each secondary interface. All four of these 72-byte FIFOs are organized as 18 x 32-bit arrays.

The APB also has 2 internal arbiters to support devices residing on each of the secondary buses.

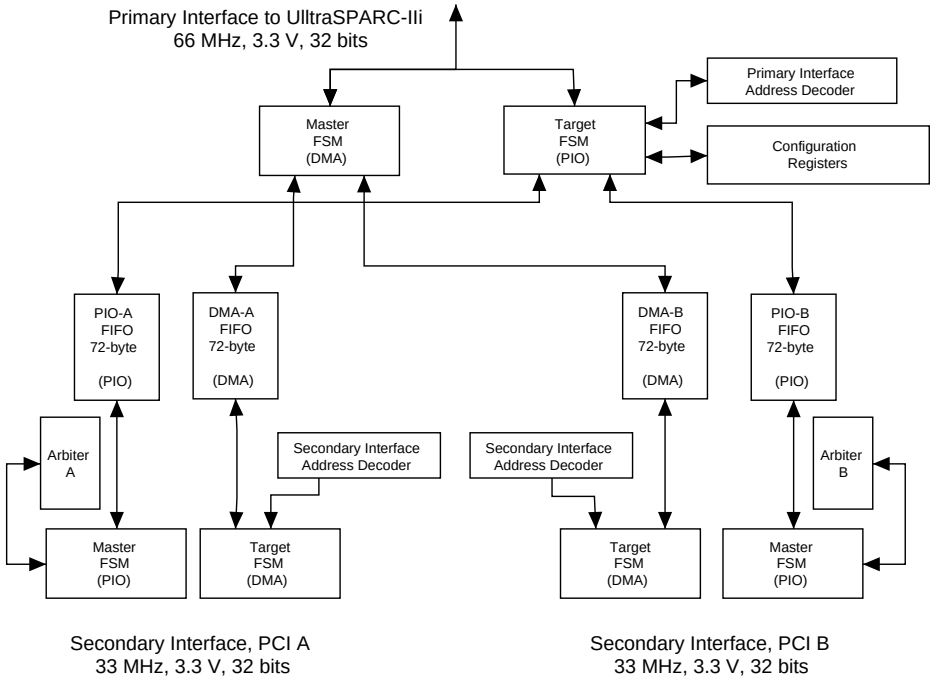


Figure 31. Advanced PCI Bridge Datapaths and Modules

Functional Overview

PCI Commands

The list below shows the commands that the Advanced PCI Bridge can generate and its response to all commands as a target.

PCI Command Generation and Response

Command	C/BE#	Generate?	Response
Interrupt Acknowledge	0000	Yes	Ignored on Secondary Buses
Special Cycle	0001	Yes (From config. cycle)	Special Cycles do not cross the bridge. No response.
I/O Read	0010	Yes	Ignored on Secondary Buses
I/O Write	0011	Yes	Ignored on Secondary Buses
Reserved	0100	No	Ignored
Reserved	0101	No	Ignored
Memory Read	0110	Yes	Perform non-prefetched read (PIO) Perform 64 byte prefetched read (DMA)
Memory Write	0111	Yes	Perform write access
Reserved	1000	No	Ignored
Reserved	1001	No	Ignored
Configuration Read	1010	Yes	Ignored on Secondary Buses
Configuration Write	1011	Yes	Ignored on Secondary Buses (except to generate special cycles or Type-1 -> Type-1)
Memory Read Multiple	1100	Yes	Perform 8 byte prefetched read (PIO). Perform 64 byte prefetched read (DMA)
Dual Address Cycle	1101	Yes. Only on Primary bus.	Receive only on Secondary Buses
Memory Read Line	1110	Yes	Perform 64 byte prefetched read (PIO) Perform 64 byte prefetched read (DMA)
Memory Write & Invalidate	1111	Yes	Equivalent to Memory Write command

Address Decoding

The APB does not use the address decoding mechanisms described in the PCI-to-PCI Bridge Architectural Specification [1]. There are two separate 8-bit address map registers, one for I/O addressing and one for memory addressing. For downstream I/O or memory transactions, the address space is divided into 8 segments. Each of these segments can be assigned to bus A, bus B, or no bus. If the three most significant bits (bits 31, 30, and 29 for memory transactions; bits 23, 22, and 21 for I/O transactions) match a segment number that is

1. All references to the PCI Bridge specification refer to *PCI to PCI Bridge Architecture Specification, Revision 1.0, April 5, 1994.*

assigned to bus A or bus B, transactions are then forwarded downstream. Upstream I/O transactions are never forwarded. Configuration transactions in both directions are treated as specified by the PCI-to-PCI bridge specification. This may present a compatibility issue. See "Exceptions to PCI Compatibility," on page 13.

All APB target units use medium decode timing. Addresses and commands are latched into APB during the address phase. In the clock after the address phase, APB decodes the transaction. If the transaction is accepted, APB asserts DEVSEL# at the next clock edge.

The PCI configuration space is 10.5 Megabytes (256 buses, 21 devices per bus, 8 functions per device, 256 bytes per function) and is accessed through PCI configuration commands. Type 0 commands refer to the bus upon which the transaction occurs. Type 0 commands carry IDSEL, function numbers, and register numbers. Type 1 commands refer to a bus other than the one where the transaction occurs and carry bus numbers, device numbers, function numbers, and register numbers. Type 0 configuration commands are not forwarded, they are used to configure the APB or other PCI devices connected to the PCI bus where the command was generated. Type 1 configuration commands can be forwarded by the APB to any level in the PCI bus hierarchy.

The Advanced PCI Bridge does not implement IDSEL pins on its secondary interfaces. Type 0 configuration commands on secondary interfaces are ignored.

Data Buffering

The APB has 72-byte data buffers for buffering of upstream and downstream transactions. These hold addresses, data, commands, and byte-enables and are used for both read and write transactions. Write transactions of all types (memory, I/O, and configuration) are posted. Strict ordering of all transactions from a particular bus to another bus (for example from primary to bus A) is maintained, but no ordering between buses is implied (in other words, primary to bus A and bus A to primary are not ordered).

The lack of ordering between PIO and DMA transactions involving the same secondary bus is not in accordance with PCI ordering rules.

Write Transactions

All write transactions are decoupled between the initiating interface and the target interface of APB. When a write transaction is received, decoded, and accepted, APB checks the status of the FIFO for the appropriate data path. If the FIFO is full or almost full and the opposite target is busy, then RETRY is signalled to the originating master to prevent deadlock. If RETRY is not immediately asserted (indicating the FIFO is not full), the address and command are placed into the FIFO.

The APB usually does not insert wait states (as a target) into write transactions. As data is received, it is posted in the FIFO. The exception is when the FIFO is full or nearly full. The APB then inserts wait states until the FIFO is less full. APB also prevents deadlocks by disconnecting the transaction if the FIFO is full or nearly full and the opposite target is busy. (See "Exceptions to PCI Compatibility," on page 13 for exceptions.)

Figure 33 depicts a write transaction.

Read Transactions

When a read transaction is received, decoded, and accepted, the APB checks the status of the FIFO for the appropriate data path. If the FIFO is full or almost full, then RETRY is signalled to the originating master. This prevents the transaction from occupying the bus when the FIFO isn't yet empty. The APB also signals RETRY when a deadlock condition is detected. (See "Deadlock Detection and Recovery," on page 10 for a more detailed discussion.) If RETRY is not immediately asserted this indicates the FIFO is not full, and the address and command are placed into the FIFO.

The APB will insert wait states into the first data phase as a target. It may also do so in subsequent data phases. A retry may be signalled after wait states in the first data phase if a deadlock occurs.

Once the destination bus master unit of APB has the bus and once the address and command are present in the FIFO, the read transaction may begin on the destination bus, unless there is a transaction ahead of it in the FIFO. At this point, handling depends on whether the transaction can be prefetched or not. This is determined by a combination of command type, direction through the APB, and the USE_PIO_PREF bits of the secondary register. A transaction is "prefetchable" as long as there are no side-effects to the read. The APB can attempt to read up to its prefetch limit without inserting wait states as a master. A disconnect is signalled to the originating master at the end of the burst of prefetched data. The prefetch buffer is cleared after every transaction.

Prefetchable reads assert all byte enables and can read locations beyond those desired. A prefetchable read must never be used in an address space where reads have side effects.

In some clock modes and directions, additional delays are added to allow parity to be correctly propagated. For both prefetchable and non-prefetchable reads, APB asserts TRDY# on the originating bus whenever data becomes available.

Reads do not pull out any posted writes in the opposite direction. *Figure 32* depicts a read transaction.

PCI Bus Arbitration

The APB contains a PCI bus arbiter for each of the two secondary PCI interfaces. Upon exiting RESET, the arbiter defaults to providing a fair arbitration scheme (round-robin) to all secondary devices. Any device, including APB, can be given priority so that it gets the bus for every other transaction.

Both arbiters can be independently disabled at reset, allowing an external arbiter to be used.

If there are no pending requests, the APB will park at the last-granted agent or at the bridge depending upon the setting of a mode bit that selects between these options.

A synchronization mechanism ensures that any transactions from non-CPU masters on PCI have been completed before an interrupt is handled. To accomplish this, the CPU asserts a DRAIN signal. While this signal is asserted, APB retries all DMA writes. The CPU continues to assert DRAIN until APB signals EMPTY (asserted when the DMA FIFOs do not contain write data and the primary master unit is not trying to continue a Retried or Disconnected write).

Deadlock Detection and Recovery

The APB contains mechanisms to avoid and to detect deadlock conditions. Deadlocks are avoided by retrying newly-received transactions that are known to cause deadlocks. In some cases, this mechanism is not sufficient and the deadlock still occurs (for example, when two transactions that deadlock each other arrive at the same time). When a deadlock is detected, one of the deadlocked transactions is retried. When avoiding or breaking a deadlock, a count of retries is maintained to prevent one bus from always being the one retried. When the count reaches a configurable limit, another transaction in the deadlock must be retried.

Error Support and Parity

Any error in a transaction, including master aborts, target aborts and parity errors, is reported by the APB in some fashion. In general, if the error can be reported in the normal course of the transaction, it is. If not, SERR# is asserted. Asynchronous fault status and address registers (AFSRs and AFAR) are provided for each datapath in the system to indicate the cause of SERR# assertion.

SERR# assertions on the secondary bus can be forwarded to the primary bus. Address parity errors result in SERR# assertion, but the transaction is otherwise handled normally. All error handling functions are enabled and disabled by command register bits as specified in the PCI and PCI Bridge specifications.

The APB usually passes along only the data and parity received from one interface to the other. However, in some cases the Advanced PCI Bridge corrects or regenerates parity.

Configuration Registers

The internal configuration space of the Advanced PCI Bridge is organized as two functions. Function 0 contains registers that pertain to transactions to or from bus A. Function 1 contains registers that pertain to transactions to or from bus B. Some registers relating to the primary bus appear in both functions. All registers can be accessed with PCI Type 0 configuration commands. Each register is defined in *Table 2*. Some registers, while listed, are not implemented in the Advanced PCI Bridge. These registers are indicated by shading in the table. Such unimplemented registers are from the PCI bridge configuration header and are not needed in APB. The rule used is that any optional register for which equivalent information exists elsewhere is not implemented.

Accessing Reserved Registers

Read accesses of reserved or unimplemented registers are completed normally and return a data value of zero. Writes to reserved registers are also completed normally, discarding write data (except for spare bits). Writes to reserved spare bits are completed with data written.

Accessing Reserved Bit Fields

Software must be careful when accessing registers which have bit fields reserved for future use. For read accesses, software must use appropriate masks to extract the defined bits and may not rely on reserved bits being any particular value. For write accesses, software must ensure that the values of reserved bit positions are preserved. That is, the current values of the reserved bit positions must be read and merged with the new values for other bit positions before the merged data is written back.

Reset Events

The assertion of the primary bus reset signal affects the state of all writable bits in the bridge configuration registers. Assertion of the secondary bus reset signals does not affect the state of any configuration bit in APB.

R/W1C Bits

Bits marked as R/W1C are reset by writing a 1 to the bit. These bits are used in status registers.

In *Table 2*, if the "Aliased" column says "Yes," the register appears *with the same values* in both functions; a write to the register in one function will affect its value in the other function. If the "Aliased" column says "No," then separate registers exist for each function.

TABLE 2: Configuration Space Summary

Register	Byte Address	Size	Aliased	Reset Value
Required PCI to PCI bridge configuration header				
Vendor ID	0x00	2 bytes	Yes	0x108E
Device ID	0x02	2 bytes	Yes	0x5000
Primary Command	0x04	2 bytes	Yes	0x0000 [1]
Primary Status	0x06	2 bytes	Yes	0x02A0
Revision ID	0x08	1 byte	Yes	0x00 [2]
Class Code	0x09	3 bytes	Yes	0x060400
Cache Line Size [3]	0x0C	1 byte	n/a	0x10
Primary Master Latency Timer	0x0D	1 byte	Yes	0x28
Header Type	0x0E	1 byte	Yes	0x81
BIST	0x0F	1 byte	n/a	0x00
Base Address	0x10	8 bytes	n/a	0x0....0
Primary Bus Number	0x18	1 byte	Yes	0x00
Secondary Bus Number	0x19	1 byte	No	0x00
Subordinate Bus Number	0x1A	1 byte	No	0x00
Secondary Master Latency Timer	0x1B	1 byte	No	0x28
IO Base	0x1C	1 byte	n/a	0x00
IO Limit	0x1D	1 byte	n/a	0x00
Secondary Status	0x1E	2 bytes	No	0x0280
Memory Base	0x20	2 bytes	n/a	0x0000
Memory Limit	0x22	2 bytes	n/a	0x0000
Prefetchable Memory Base	0x24	2 bytes	n/a	0x0000
Prefetchable Memory Limit	0x26	2 bytes	n/a	0x0000
Prefetchable Base Upper 32bits	0x28	4 bytes	n/a	0x0000.0000
Prefetchable Limit Upper 32 bits	0x2C	4 bytes	n/a	0x0000.0000
I/O Base Upper 16 bits	0x30	2 bytes	n/a	0x0000
I/O Limit Upper 16 bits	0x32	2 bytes	n/a	0x0000
Reserved	0x34	4 bytes	n/a	0x0000.0000
Expansion ROM Base address	0x38	4 bytes	n/a	0x0000.0000
Interrupt Line	0x3C	1 byte	n/a	0x00
Interrupt pin	0x3D	1 byte	n/a	0x00

TABLE 2: Configuration Space Summary

Register	Byte Address	Size	Aliased	Reset Value
Bridge Control	0x3E	2 bytes	No	0x0000
Device specific registers				
Reserved (unused)	0x40 - 0xAF	112 bytes	n/a	0x00....
Tick Register	0xB0	4 bytes	Yes	0x0000.0000 [4]
Reserved (unused)	0xB4-0xB7	4 bytes	n/a	0x00....
INT ACK generation register	0xB8	4 bytes	No	n/a
Reserved (unused)	0xBC-0xBF	4 bytes	n/a	0x00....
Primary Master Retry Limit	C0	1 byte	Yes	0x00
Reserved (unused)	0xC1 - C7	7 bytes	n/a	0x00....
DMA AFSR	0xC8	8 bytes	No	0x00..00
DMA AFAR	0xD0	8 bytes	No	0x00..00
PIO Target Retry Limit	0xD8	1 byte	No	0x00
PIO Target Latency Timer	0xD9	1 byte	No	0x00
DMA Target Retry Limit	0xDA	1 byte	No	0x00
DMA Target Latency Timer	0xDB	1 byte	No	0x00
Secondary Master Retry Limit	0xDC	1 byte	No	0x00
Secondary Control Register	0xDD	1 byte	No	0x00
I/O Address Map Register	0xDE	1 byte	No	0x00
Memory Address Map Register	0xDF	1 byte	No	0x00 [5]
Other registers				
PCI Control Register	0xE0	8 bytes	No	0x00..00 [6]
PIO AFSR	0xE8	8 bytes	No	0x00..00
PIO AFAR	0xF0	8 bytes	No	0x00..00
Device specific register				
Diagnostic Register	0xF8	8 bytes	No	0x00..00

1. If the Boot pin is tied high, the reset value of the Command Register is 0x0002.
2. This will vary with different revisions of APB.
3. Shading indicates optional registers in the PCI bridge configuration header. The registers so indicated have not been implemented because equivalent information exists elsewhere in the system.
4. The Tick begins counting immediately after reset.
5. If the Boot pin is tied high, the reset value of Memory Address Map Register B is 0xFF.
6. Resets to 0x0001.0000.0000.0000 in 1:1 clock mode.

PCI Optional Features Not Implemented

The following optional features of the PCI specification have not been implemented:

- Addressing modes other than linear are disconnected with the first data phase
- No LOCK# pin signal is used
- Clock stopping is not available
- Cache support pins are not needed
- No DOS compatibility features have been added
- Memory write-and-invalidate transactions are treated as memory-write
- APB does not generate fast back-to-back cycles as master
- APB does not step addresses or data
- APB does not provide VGA support

Exceptions to PCI Compatibility

The following exceptions to PCI compatibility are in place:

- In general, if the destination bus target does not insert wait states and the buses are idle when a transaction begins, the latency target guideline is met. For write cycles, the latency guideline is met unless the FIFO becomes full during the transaction. However, 16-clock initial and 8-clock subsequent TRDY# latency are not always met. For read cycles, TRDY# latency depends on the speed of the destination bus target and the clock mode.
- In general, if the destination bus target does not insert wait states and the buses are idle when a transaction begins, the master (IRDY#) latency target guideline is met. For read cycles, IRDY# latency depends on the clock mode, the number of wait states inserted by the target, and the number of wait states inserted by the master. For write cycles, the latency depends on the clock mode and the number of wait states inserted by the master. If the master inserts no wait states, the latency guideline is met.
- The Base and Limit registers defined by the PCI Bridge Specification are not implemented.
- The Primary Master Latency Timer and Secondary Master Latency Timer registers are initialized to 0x28 instead of 0x00. This ensures internal consistency.
- Both I/O write transactions and configuration write transactions are posted.
- The Memory Read Multiple command prefetches less than a cache line.
- PCI Ordering rules are not followed. While all transactions originating on a particular bus are ordered, there is no ordering between buses. In particular, a read does not “pull out” any posted writes in the opposite direction. The producer-consumer model is, to this degree, not followed. See the relevant Appendix of the PCI 2.1 specification for more information about ordering rules.

SIGNAL DESCRIPTION

Primary PCI Bus Interface

PIN NAME	Qty	I/O	Assertion	DESCRIPTION
AD[31:00]	32	I/O	High	Address and Data
C/BE[3:0]#	4	I/O	Low	Bus Command and Byte Enables
Devsel#	1	I/O	Low	Device select
Frame#	1	I/O	Low	Cycle Frame-to indicate beginning of an access
Gnt#	1	I	Low	Bridge is granted the usage of PCI bus
Idsel	1	I	High	Initialization device select
Irdy#	1	I/O	Low	Initiator ready
Par	1	I/O	High	Parity-even
Perr#	1	I/O	Low	Parity error
Rst#	1	I	Low	Reset
Clk	1	I	High	Clock input - 66MHz
Stop#	1	I/O	Low	Stop request by target
Trdy#	1	I/O	Low	Target ready
Req#	1	O	Low	Request for usage of PCI bus by bridge
Serr#	1	O	Low	System error

Secondary PCI Bus Interfaces

PIN NAME	Qty	I/O	Assertion	DESCRIPTION
A_AD	32	I/O	High	Address and Data - PCI Bus A
A_C/BE#	4	I/O	Low	Bus Command/Byte Enables - PCI Bus A
A_Devsel#	1	I/O	Low	Device select - PCI Bus A
A_Frame#	1	I/O	Low	Cycle Frame-to indicate beginning of an access - PCI Bus A
A_Gnt[0]#	1	I/O	Low	Internal PCI arbiter enabled - Output Internal PCI arbiter disabled - Input
A_Gnt[3:1]#	3	O	Low	PCI Grant[3:1] - PCI Bus A
A_Irdy#	1	I/O	Low	Initiator ready - PCI Bus A
A_Par	1	I/O	High	Parity-even - PCI Bus A
A_Perr#	1	I/O	Low	Parity error - PCI Bus A
A_Rst#	1	O	Low	Reset - PCI Bus A
A_Stop#	1	I/O	Low	Stop request by target - PCI Bus A
A_Trdy#	1	I/O	Low	Target ready - PCI Bus A
A_Req[0]#	1	I/O	Low	Internal PCI arbiter enabled - Input Internal PCI arbiter disabled - Output
A_Req[3:1]#	3	I	Low	PCI Request[3:1] - PCI Bus A
A_Serr#	1	I/O	Low	System error - PCI Bus A

Secondary PCI Bus Interfaces (Continued)

PIN NAME	Qty	I/O	Assertion	DESCRIPTION
B_AD	32	I/O	High	Address and Data - PCI Bus B
B_C/BE#	4	I/O	Low	Bus Command/Byte Enables - PCI Bus B
B_Devsel#	1	I/O	Low	Device select - PCI Bus B
B_Frame#	1	I/O	Low	Cycle Frame-to indicate beginning of an access - PCI Bus B
B_Gnt[0]#	1	I/O	Low	Internal PCI arbiter enabled - Output Internal PCI arbiter disabled - Input
B_Gnt[3:1]#	3	O	Low	PCI Grant[3:1] - PCI Bus B
B_Irdy#	1	I/O	Low	Initiator ready - PCI Bus B
B_Par	1	I/O	High	Parity-even - PCI Bus B
B_Perr#	1	I/O	Low	Parity error - PCI Bus B
B_Rst#	1	O	Low	Reset - PCI Bus B
B_Stop#	1	I/O	Low	Stop request by target - PCI Bus B
B_Trdy#	1	I/O	Low	Target ready - PCI Bus B
B_Req[0]#	1	I/O	Low	Internal PCI arbiter enabled - Input Internal PCI arbiter disabled - Output
B_Req[3:1]#	3	I	Low	PCI Request[3:1] - PCI Bus B
B_Serr#	1	I/O	Low	System error - PCI Bus B

Other Control Pins

PIN NAME	Qty	I/O	Assertion	DESCRIPTION
Clk_33	1	I	High	33 MHz PCI clock
Boot	1	I	High	Boot PROM is behind APB bus B
EMPTY	1	O	High	To UltraSPARC-II*i* for signalling there are no DMA stores inside APB
DRAIN	1	I	High	From UltraSPARC-II*i* signalling request to drain the DMA stores.
PLL Support Pin	7	-	-	-
5V VDD	14	-	-	-
3.3V VDD	12	-	-	-
GND	29	-	-	-
NC	44	-	-	-

Test pins

PIN NAME	Qty	I/O	Assertion	DESCRIPTION
TDI	1	I	High	Test Data Input (JTAG)
TDO	1	O	High	Test Data Output (JTAG)
TCK	1	I	High	Test clock (JTAG)
TMS	1	I	High	Test Mode Select (JTAG)
TN	1	I	Low	Three-states all bidirectional pads
MTEST	1	I	-	Manufacturing Test Output
TRST#	1	I	Low	Test reset (JTAG)
TOTAL PINS	272	-	-	-

TIMING INFORMATION

PCI Read

Figure 32 illustrates a read transaction. For more information, see the relevant section of the PCI Specification.

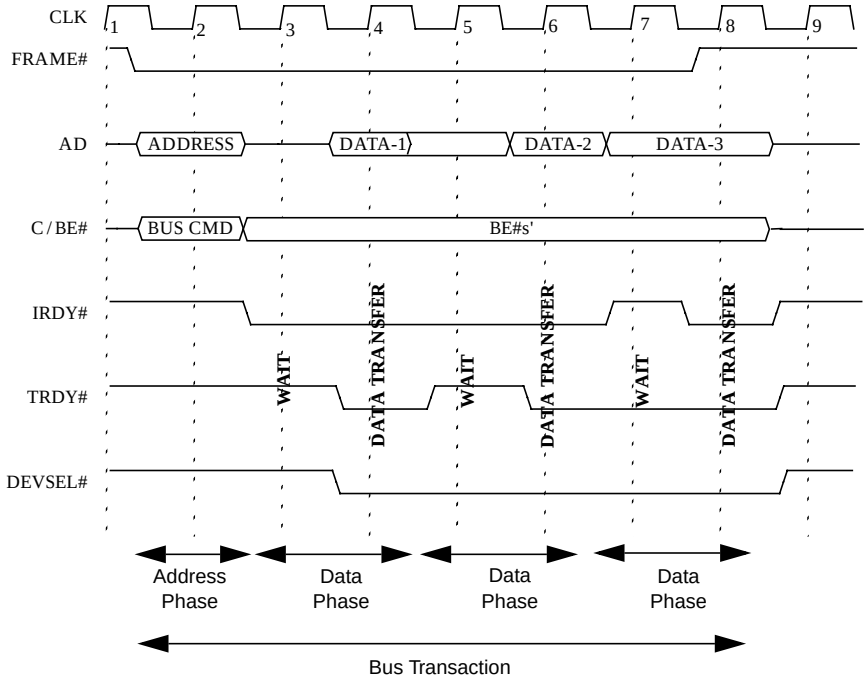


Figure 32. Basic PCI Read Operation

Note: Wait states and DEVSEL# timing may vary.

PCI Write

Figure 33 illustrates a write transaction. For more information, see the relevant section of the PCI Specification.

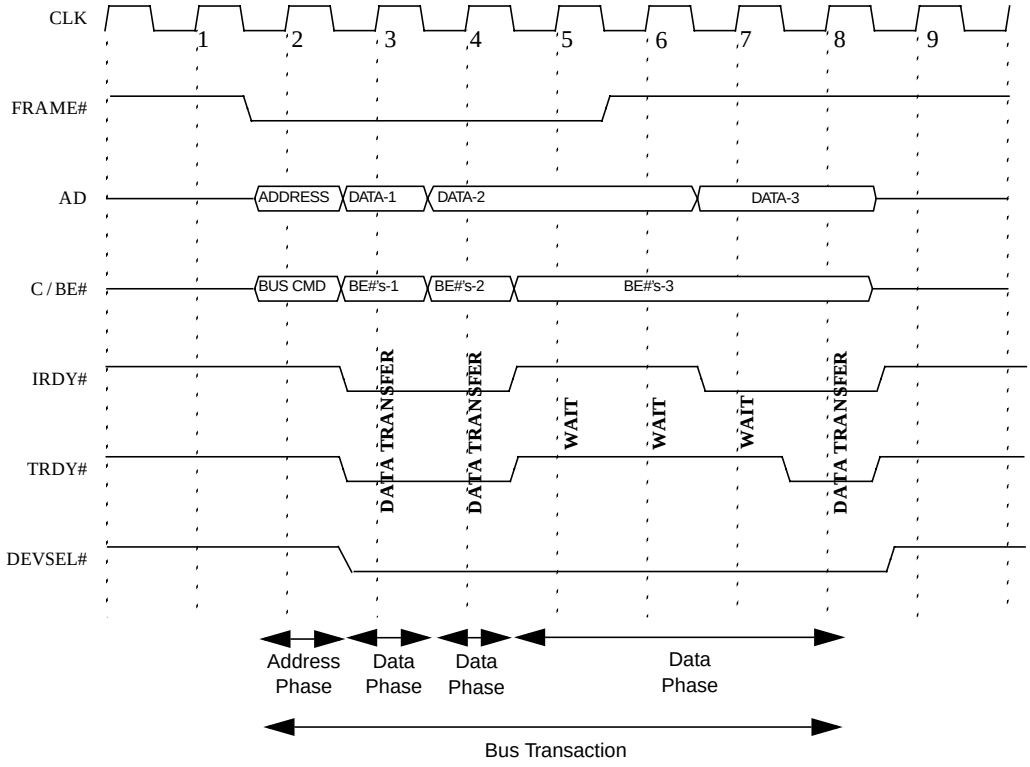


Figure 33. Basic PCI Write Operation

Note: Wait states and DEVSEL# timing may vary.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Rating

Symbol	Parameter	Rating [1]	Unit
V_{DD}	DC Supply Voltage	-0.3 to + 3.9	V
V_{IN} [2]	Input Voltage	-1.0 to V_{DD} + 0.3	V
V_{IN2} [2]	Secondary Interface Input Voltage	-1.0 to 6.5	V
I_{IN}	DC Input Current	± 10	mA
T_{STG}	Storage Temperature Range (Plastic) [3]	-40 to + 125	° C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operation conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Inputs should not reach or exceed 3.3 V until 3.3 V rail has exceeded 3 V.
3. Units are JEDEC level III moisture sensitive and will be shipped dry packed from supplier. Unit assembly should occur on PCB within 72 hours after removal from dry pack. Pieces not assembled within this time fence must be baked in a nitrogen environment at 125C before reflow operation. If the sealed product packaging is opened in a humid environment, units must be reflowed quickly per JEDEC spec or must be baked to drive out any absorbed moisture.

Recommended Operating Conditions

Symbol	Parameter [1]	Min	Nom	Max	Unit
V_{DD} [2]	DC Supply Voltage	+ 2.15	3.3	3.6	V
V_{DD5} [2]	5V Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	-	70	°C
T_J	Junction Temperature	-	-	150	°C

1. For normal device operation, adhere to the limits in this table. Sustained operation of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, may result in permanent device damage or impaired device reliability. Device functionality to stated DC and AC limits is not guaranteed if conditions exceed recommended operating conditions.
2. 3.3 V Rail should not exceed 5 V rail by more than 1 V for more than 100 ms unless RST_1 is asserted.

Interface Signal DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input Voltage High, Primary Bus		0.475 * V_{DD}	V_{DD} + 0.5	V
	Input Voltage High, Secondary Bus	3.3 V Signalling	0.475 * V_{DD}	V_{DD} + 0.5	V
	Input Voltage High, CLK	5 V Signalling	2.0	V_{DD} + 0.5	V
	Input Voltage High, Other Pins		2.0	5.5	V
V_{IL}	Input Voltage Low, Primary Bus		-0.5 V	0.325 * V_{DD}	V
	Input Voltage Low, Secondary Bus	3.3 V Signalling	-0.5 V	0.325 * V_{DD}	V
	Input Voltage Low, Secondary Bus	5 V Signalling	-0.5 V	0.325 * V_{DD}	V
	Input Voltage Low, Other Pins		-0.5 V	0.8	V
I_{IH}	Input Leakage Current High	V_{IN} = V_{DD}	-	+10	µA
I_{IL}	Input Leakage Current Low	V_{IN} = V_{SS}	-10	-	µA
V_{OH}	Output Voltage High, Primary Bus	I_{OH} = -500 µA	0.9 * V_{DD}	V_{DD} + 0.5	V
	Output Voltage High, Secondary Bus	I_{OH} = -500 µA 3.3 V Signalling	0.9 * V_{DD}	-	V
	Output Voltage High, Secondary Bus	I_{OH} = -12 mA 5 V Signalling	2.4	-	V
	Output Voltage High, Other Pins	I_{OH} = -4 mA	2.4	V_{DD}	V
V_{OL}	Output Voltage Low, Primary Bus	I_{OL} = 500 µA	-	0.1 * V_{DD}	V
	Output Voltage Low, Secondary Bus	I_{OL} = 1500 µA 3.3 V Signalling	-	0.1 * V_{DD}	V
	Output Voltage Low, Secondary Bus	I_{OL} = 12 mA 5 V Signalling	-	0.55	V
	Output Voltage Low, Other Pins	I_{OL} = 4 mA	-	0.4	V
I_{OH}	Output Current at High State, Primary Bus	V_{OH} = 2.4 V	-	-6	mA
	Output Current at High State, Secondary Bus		-	-12	mA
	Output Current at High State, Other Pins		-	-4	mA
I_{OL}	Output Current at Low State, Primary Bus	V_{OL} = 0.4 V	6	-	mA
	Output Current at Low State, Secondary Bus		12	-	mA
	Output Current at Low State, Other Pins		4	-	mA
I_{OZ}	3-State Leakage Current	V_O = V_{DD} or V_{SS}	-10	10	µA
P_D	Power Dissipation		-	3.5	W
C_{IN}	Input Capacitance, Primary Bus		-	3.1	pF
	Input Capacitance, Secondary Bus		-	3.1	pF
	Input Capacitance, Clk		-	3.0	pF

Interface Signal DC Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance, Other Pins		-	4.38	pF
C_{OUT}	Output Capacitance, Primary Bus		-	4.98	pF
	Output Capacitance, Secondary Bus		-	4.98	pF
	Output Capacitance, Other Pins		-	3.88	pF

PCI Interface Signal AC Characteristics

Symbol	Parameter [1]	Conditions	Min	Max	Unit
$I_{OH(AC)}$	Switching Current High, Primary/Secondary Bus	$0.3 * V_{DD}$	-36 [1]	-	mA
	Switching Current High, Primary/Secondary Bus	$0.7 * V_{DD}$	-	-115[1]	mA
$I_{OL(AC)}$	Switching Current Low, Primary/Secondary Bus	$0.6 * V_{DD}$	48	-	mA
	Switching Current Low, Primary/Secondary Bus	$0.18 * V_{DD}$	-	137	mA
t_R	Output Rise Slew Rate, Primary Bus	$0.3 * V_{DD}$ to $0.6 * V_{DD}$	2.0	6.0	V/ns
	Output Rise Slew Rate, Secondary Bus	0.4 to 2.4 V	1.1	3.5	V/ns
t_F	Output Rise Slew Rate, Primary Bus	$0.6 * V_{DD}$ to $0.3 * V_{DD}$	2.4	5.9	V/ns
	Output Rise Slew Rate, Secondary Bus	0.4 V to 2.4 V	0.8	4.2	V/ns
I_{CL}	Low Clamp Current, Primary Bus	$-3 < V_{IN} < -1$ V	$-25 + (V_{IN}+1)/ 0.015$ [2]	-	mA
	Low Clamp Current, Secondary Bus	$-5 < V_{IN} < -1$ V	$-25 + (V_{IN}+1)/ 0.015$(2)	-	mA
I_{CH}	High Clamp Current, Primary Bus	$V_{DD}+ 4V > V_{IN} > V_{DD}+ 1V$	$25 + (V_{IN}-V_{DD} - 1)/ 0.015$	-	mA

1. See V/I Curves in the PCI Specification.
2. Negative minimum current values imply that current may be created in the negative direction.

Timing Specifications

Test Conditions

Parameter	Condition
Junction Temperature	0 - 105 °C
DC Supply Voltage	3.0 - 3.6 V
5V Voltage	4.75 - 5.25 V
Process models	fast / fast to slow / slow
Output loading - PCI buses - empty - tdo	 See PCI Specification 10 pF 70 pF
Input Slew Rate	See PCI Specification
Input waveforms	See *Table 3*

Clock/Reset AC Timing

Symbol	Parameter	Notes/Conditions	Min	Max	Unit
F_P	Primary Clock Frequency	- [1]	0	66	MHz
T_{P_CYC}	Primary Clock Cycle Time	-	15	-	ns
T_{P_HIGH}	Primary Clock High Time	-	6	-	ns
T_{P_LOW}	Primary Clock Low Time	-	6	-	ns
T_{P_SLEW}	Primary Clock Slew Rate	-	1.5	4	V/ns
F_S	Secondary Clock Frequency	- [2]	-	33	MHz
T_{S_CYC}	Secondary Clock Cycle Time	-	30	-	ns
T_{S_HIGH}	Secondary Clock High Time	-	11	-	ns
T_{S_LOW}	Secondary Clock Low Time	-	11	-	ns
T_{S_SLEW}	Secondary Clock Slew Rate	-	1	4	V/ns
T_{SKEW}	Primary to Secondary Clock Skew	- [3]	-2	2	ns
T_{SU_CLK}	Secondary Clock Set Up Time [4]	PLL bypassed	0.75	-	ns
	Secondary Clock Set Up Time[4]	PLL enabled	0.75	-	ns
T_{HOLD_CLK}	Secondary Clock Hold Time[4]	PLL bypassed	0.75	-	ns
	Secondary Clock Hold Time[4]	PLL enabled	0.75	-	ns
F_{PLL}	PLL Range	- [5]	30	70	MHz
T_{LOCK}	PLL Lock Time	-	1	-	ms
T_{RST}	Reset active time after power stable	-	1	-	ms
T_{RST_CLK}	Reset active time after clock stable	-	100	-	µs
T_{RST_OFF}	Reset active time to output float delay	-	-	40	ns

1. Clock may be varied dynamically at frequencies below 33 MHz. At frequencies above 33 MHz, RST# must be asserted before changing frequency.
2. Secondary clock frequency must be either 1/2 of the primary clock frequency or equal the primary clock frequency. If secondary and primary clock frequencies are to be equal, the CLK_33 input should be tied high or low.
3. Skew is measured between the rising edges of the two clocks. There must be no more than 2 ns absolute skew between the rising edges of the primary clock input pin and the secondary clock input pin of ANY device on a secondary bus.
4. Secondary clock setup and hold time is referenced to the negative edge of the primary clock if the PLL is disabled, or 1/2 the primary clock cycle time +/- 5% if the PLL is enabled. These setup and hold times will constrain secondary and primary clock high and low times. Secondary clock transitions must not occur within the following guardbands:

PLL Disabled: from (Tp-high - Tsu-clk) to (Tp-high + Thold-clk)

PLL Enabled: from (Tp-cyc * 0.45 - Tsu-clk) to {(Tp-cyc * 0.55) + Thold-clk}

Note that secondary clock transitions will take place at:

Ts-high + Tskew, Ts-low + Tskew, Ts-cyc - Ts-high - Tskew, and Ts-cyc - Ts-low - Tskew

A 50% duty cycle on both clocks will always meet these requirements. Also, a 66 MHz primary clock and a 33 MHz secondary clock meeting the minimum high and low times given in the table will meet these requirements.

5. PLL must be enabled when primary clock frequency >= 33 MHz. PLL must be disabled when primary clock frequency < 33 MHz.

TIMING PARAMETERS

Clock/Reset AC Timing

Symbol	Parameter	Notes/Conditions	Min	Max	Unit
T_{VAL}	Clock to signal-valid delay, primary signals (including. empty)	PLL Enabled	1	6	ns
	Clock to signal-valid delay, primary signals (including. empty)	PLL Disabled	2	11	ns
	Clock to signal-valid delay, secondary bussed signals		2	11	ns
	Clock to signal-valid Delay, Secondary req#/gnt#		2	12	ns
T_{ON}	Float to active delay, primary signals	PLL Enabled	1	-	ns
	Float to active delay, primary signals	PLL Disabled	2	-	ns
	Float to active delay, secondary signals		2	-	ns
T_{OFF}	Active to float delay, primary signals	PLL Enabled	-	14	ns
	Active to float delay, primary signals	PLL Disabled	-	28	ns
	Active to float delay, secondary signals		-	28	ns
T_{SU}	Input set up time to clock, primary signals (including drain)	PLL Enabled	5	-	ns
	Input set up time to clock, primary signals (including drain)	PLL Disabled	7	-	ns
	Input set up time to clock, secondary bussed signals		7	-	ns
	Input set up time to clock, secondary req#		12	-	ns
	Input set up time to clock, secondary gnt#		10	-	ns
T_{HOLD}	Input hold time from clock		0	-	ns

PARAMETER MEASUREMENT

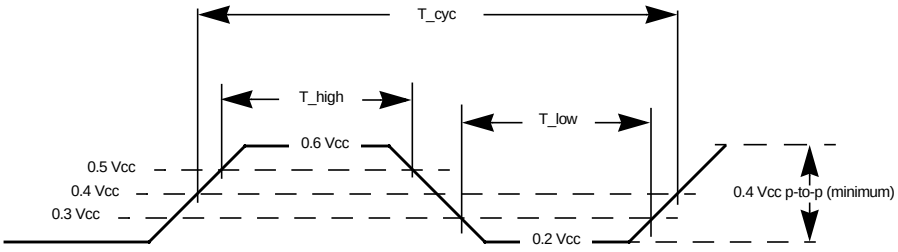


Figure 34. 3.3 V Clock Waveform

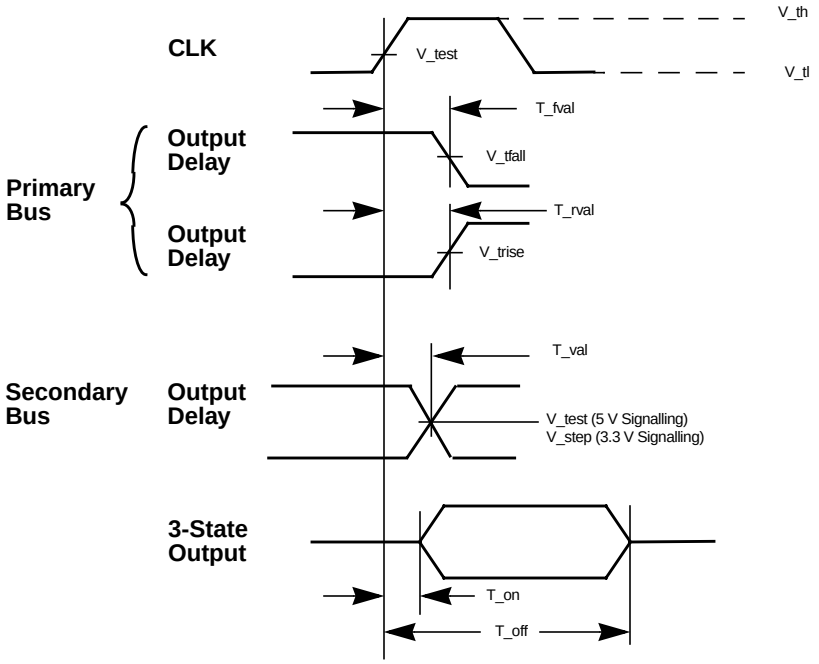


Figure 35. Output Timing Measurement Conditions

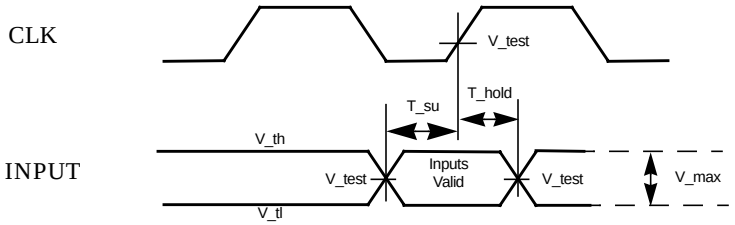


Figure 36. Input Timing Measurement Conditions

TABLE 3: Measurement Condition Parameters

Symbol	5 V Signaling	3.3 V Signaling	Units
V_{TH}	2.4	0.6 V_{CC}	V [1]
V_{TL}	0.4	0.2 V_{CC}	V [1]
V_{TEST}	1.5	0.4 V_{CC}	V
V_{STEP} (rising edge)	n/a	0.285 V_{CC}	V
V_{MAX}	2.0	0.4 V_{CC}	V [2]
Input Signal Edge Rate	1 V/ns		
V_{STEP} (falling edge)	n/a	0.615 V_{CC}	V
V_{TRISE}	n/a	0.285 V_{CC} [3]	V
V_{TFALL}	n/a	0.615 V_{CC}0	V

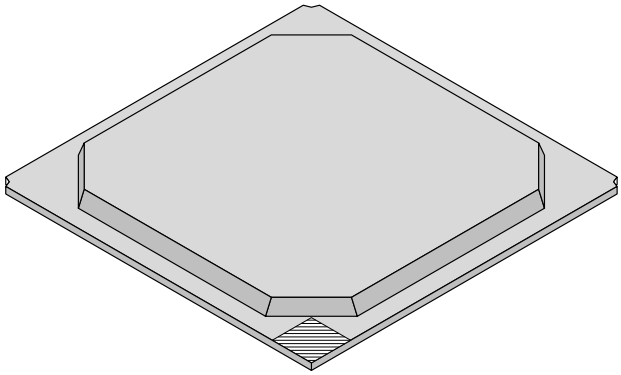
1. The input test for the 5 V environment is done with 400 mV of overdrive (over VIH and VIL); the test for the 3.3 V environment is done with 0.1 VCC of overdrive. Timing parameters must be met with no more overdrive than this.
2. VMAX specifies the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to the parameters in *Table 3*.
3. V_{TRISE} and V_{TFALL} are reference voltages for timing measurements only.Developers of 66 MHz PCI systems need to design buffers that launch enough energy into a 25 Ohm transmission line so that correct input levels are guaranteed after the first reflection.

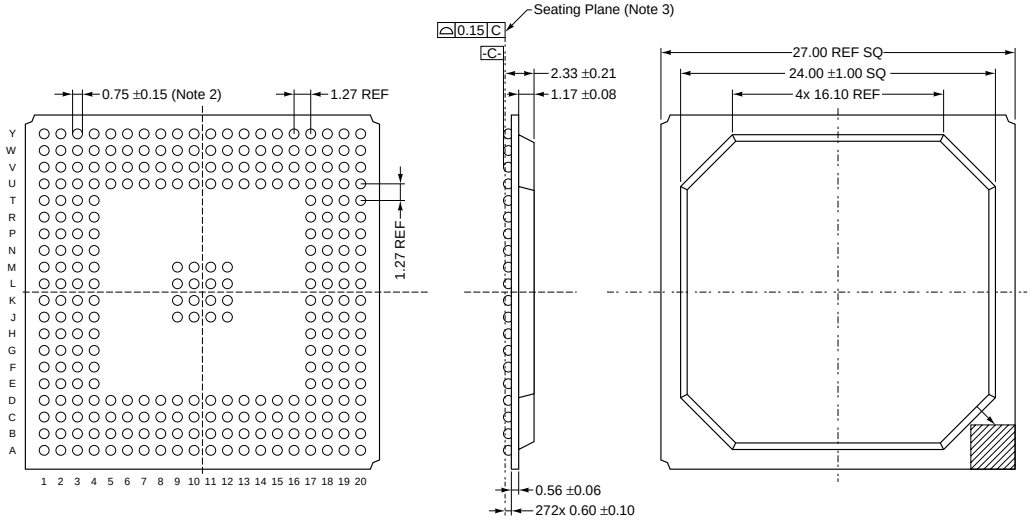
272 PBGA Pin Assignment

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
A1	VSS	D9	Rst#	L1	AD[10]	U13	GND
A2	Idsel	D10	NC	L2	AD[9]	U14	A_Req[1]#
A3	NC	D11	3.3V VDD	L3	AD[8]	U15	3.3V VDD
A4	AD[25]	D12	pllbias	L4	C/BE[0]#	U16	A_Gnt[1]#
A5	AD[28]	D13	GND	L9	GND	U17	GND
A6	AD[31]	D14	B_Gnt[0]#	L10	GND	U18	B_AD[2]
A7	Gnt#	D15	3.3V VDD	L11	GND	U19	B_AD[1]
A8	tn	D16	B_Req[1]#	L12	GND	U20	B_AD[4]
A9	Boot	D17	GND	L17	3.3V VDD	V1	A_AD[6]
A10	TCK	D18	B_AD[26]	L18	B_C/BE[1]#	V2	A_C/BE[0]#
A11	TDO	D19	B_AD[24]	L19	5V VDD	V3	A_AD[8]
A12	mtest	D20	B_C/BE[3]#	L20	B_Par	V4	NC
A13	plllp2	E1	C/BE[2]#	M1	AD[7]	V5	A_AD[14]
A14	Clk	E2	AD[16]	M2	AD[6]	V6	A_C/BE[1]#
A15	B_Gnt[2]#	E3	NC	M3	AD[5]	V7	A_Perr#
A16	B_Rst#	E4	NC	M4	AD[4]	V8	A_Trdy#
A17	B_Req[2]#	E17	NC	M9	GND	V9	A_C/BE[2]#
A18	NC	E18	NC	M10	GND	V10	A_AD[17]
A19	NC	E19	B_AD[23]	M11	GND	V11	A_AD[21]
A20	NC	E20	5V VDD	M12	GND	V12	5V VDD
B1	AD[21]	F1	Trdy#	M17	B_AD[13]	V13	A_AD[27]
B2	C/BE[3]#	F2	Irdy#	M18	B_AD[14]	V14	A_AD[31]
B3	AD[23]	F3	NC	M19	NC	V15	A_Req[2]#
B4	NC	F4	3.3V VDD	M20	B_AD[15]	V16	NC
B5	AD[26]	F17	3.3V VDD	N1	NC	V17	NC
B6	AD[29]	F18	NC	N2	AD[3]	V18	NC
B7	Req#	F19	B_AD[21]	N3	AD[2]	V19	5V VDD
B8	DRAIN	F20	B_AD[20]	N4	GND	V20	NC
B9	NC	G1	Perr#	N17	GND	W1	NC
B10	TMS	G2	Stop#	N18	NC	W2	A_AD[9]
B11	plliddtn	G3	Devsel#	N19	B_AD[11]	W3	A_AD[10]
B12	pllen	G4	Frame#	N20	B_AD[12]	W4	A_AD[11]
B13	pllagnd	G17	B_AD[22]	P1	AD[1]	W5	A_AD[15]
B14	NC	G18	NC	P2	AD[0]	W6	A_Serr#
B15	B_Gnt[1]#	G19	B_AD[19]	P3	A_AD[0]	W7	A_Stop#
B16	B_Req[3]#	G20	B_AD[18]	P4	A_AD[2]	W8	A_Irdy#
B17	B_AD[31]	H1	Par	P17	B_C/BE[0]#	W9	NC
B18	B_AD[30]	H2	Serr#	P18	NC	W10	5V VDD
B19	B_AD[29]	H3	NC	P19	B_AD[9]	W11	A_AD[20]
B20	B_AD[28]	H4	GND	P20	B_AD[10]	W12	A_C/BE[3]#
C1	AD[18]	H17	GND	R1	NC	W13	A_AD[26]
C2	NC	H18	B_AD[17]	R2	A_AD[1]	W14	A_AD[29]
C3	AD[22]	H19	B_AD[16]	R3	A_AD[3]	W15	5V VDD
C4	AD[24]	H20	B_C/BE[2]#	R4	3.3V VDD	W16	A_Req[3]#
C5	NC	J1	AD[14]	R17	3.3V VDD	W17	NC
C6	NC	J2	NC	R18	B_AD[7]	W18	A_Gnt[2]#
C7	AD[30]	J3	AD[15]	R19	5V VDD	W19	A_Gnt[3]#

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
C8	EMPTY	J4	C/BE[1]#	R20	B_AD[8]	W20	B_AD[0]
C9	TRST#	J9	GND	T1	NC	Y1	NC
C10	Clk_33	J10	GND	T2	5V VDD	Y2	5V VDD
C11	TDI	J11	GND	T3	NC	Y3	A_AD[13]
C12	pllvss	J12	GND	T4	NC	Y4	NC
C13	pllvdd	J17	B_Frame#	T17	B_AD[3]	Y5	NC
C14	B_Gnt[3]#	J18	5V VDD	T18	B_AD[5]	Y6	5V VDD
C15	5V VDD	J19	B_Irdy#	T19	NC	Y7	A_Devsel#
C16	NC	J20	B_Trdy#	T20	B_AD[6]	Y8	NC
C17	B_Req[0]#	K1	AD[11]	U1	A_AD[4]	Y9	A_AD[16]
C18	5V VDD	K2	AD[13]	U2	A_AD[5]	Y10	A_AD[18]
C19	B_AD[27]	K3	AD[12]	U3	A_AD[7]	Y11	A_AD[19]
C20	B_AD[25]	K4	3.3V VDD	U4	GND	Y12	A_AD[23]
D1	AD[17]	K9	GND	U5	A_AD[12]	Y13	A_AD[25]
D2	AD[20]	K10	GND	U6	3.3V VDD	Y14	A_AD[28]
D3	AD[19]	K11	GND	U7	A_Par	Y15	A_AD[30]
D4	GND	K12	GND	U8	GND	Y16	A_Req[0]#
D5	NC	K17	B_Devsel#	U9	A_Frame#	Y17	A_Rst#
D6	3.3V VDD	K18	B_Stop#	U10	3.3V VDD	Y18	A_Gnt[0]#
D7	AD[27]	K19	B_Perr#	U11	A_AD[22]	Y19	5V VDD
D8	GND	K20	B_Serr#	U12	A_AD[24]	Y20	NC

256 PBGA Package Information





Notes: 1. Dimensions in mm.
2. Measured at maximum solder ball diameter parallel to primary datum -C-.
3. Primary datum -C- and seating plane are defined by the spherical crowns of the solder balls.

ORDERING INFORMATION

Marketing Part No.	Speed	Description
Please contact your Sun representative for planned availability	One 66 MHz Primary and Two 33 MHz Secondary Interfaces	UltraSPARC-II*i* Advanced PCI Bridge

Document Part Number: 805-0088-02